Amendments to the Claims

Please cancel Claims 28, 36 and 44. Please amend Claims 27 and 42. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1-26. (Cancelled)

27. (Currently amended) A computer implemented method for generating machine instructions including memory access monitoring instructions, said method comprising the steps of:

receiving as input a first set of machine instructions, said first set of machine instructions being specific to a computer processor with each machine instruction of said first set corresponding to an instruction executable by said computer processor, said first set of machine instructions including a memory access instruction; and

generating a second set of machine instructions from said first set of machine instructions having additional machine instructions that are memory monitoring instructions, said memory monitoring instructions checking a memory status of a memory location accessed by said memory access instruction in conjunction with execution of said memory[[_]]access instruction, said memory status including an allocated state.

28. (Cancelled)

29. (Previously presented) The method of claim 27, wherein said allocated state includes an allocated-and-uninitialized state and an allocated-and-initialized state.

30. (Previously presented) The method of claim 29, further comprising the step of signaling an error if said memory access instruction is a read operation and said memory status indicates said memory location is in an allocated-and-uninitialized state.

31. (Previously presented) The method of claim 27, further comprising the step of maintaining said memory status for said memory location.

32. (Previously presented) The method of claim 27, wherein said second set of machine instructions has additional memory monitoring instructions for substantially all memory access instructions that access a region of memory.

33. (Previously presented) The method of claim 27, wherein said first and second set of machine instructions are object code.

34. (Previously presented) A computer program product that generates machine instructions including memory access monitoring instructions, comprising:

computer code that receives as input a first set of machine instructions, said first set of machine instructions being specific to a computer processor with each machine instruction of said first set corresponding to an instruction executable by said computer processor, said first set of machine instructions including a memory access instruction;

computer code that generates a second set of machine instructions from said first set of machine instructions having additional machine instructions that are memory monitoring instructions, said memory monitoring instructions checking a memory status of a memory location accessed by said memory access instruction in conjunction with execution of said memory access instruction, said memory status including an allocated state; and

a computer readable medium that stores said computer codes.

35. (Previously presented) The computer program product of claim 34, wherein said computer readable medium is a computer memory.

36. (Cancelled)

37. (Previously presented) The computer program product of claim 34, wherein said allocated state includes an allocated-and uninitialized state and an allocated-and-initialized state.

38. (Previously presented) The computer program product of claim 37, further comprising computer code that signals an error if said memory access instruction is a read operation and said memory status indicates said memory location is in an allocated-and-uninitialized state.

39. (Previously presented) The computer program product of claim 34, wherein said memory status is maintained for said memory location.

40. (Previously presented) The computer program product of claim 34, wherein said second set of machine instructions has additional memory monitoring instructions for substantially all memory access instructions that access a region of memory.

41. (Previously presented) The computer program product of claim 34, wherein said first and second set of machine instructions are object code.

42. (Currently amended) A computer system [[the]] that generates machine instructions including memory access monitoring instructions, comprising:

a processor; and

a storage medium coupled to said processor, said storage medium storing computer code including:

computer code that receives as input a first set of machine instructions, said first set of machine instructions being specific to a computer processor with each machine instruction of said first set corresponding to an instruction executable by said computer processor, said first set of machine instructions including a memory access instruction; and

computer code that generates a second set of machine instructions from said first set of machine instructions having additional machine instructions that are memory monitoring instructions, said memory monitoring instructions checking a memory status of a memory location accessed by said memory access instruction in conjunction with execution of said memory access instruction, said memory status ~~includes~~ including an allocated state.

43. (Previously presented) The computer system of claim 42, wherein said computer storage medium is a computer memory.

44. (Cancelled)

45. (Previously presented) The computer system of claim 42, wherein said allocated state includes an allocated-and-uninitialized state and an allocated-and-initialized state.

46. (Previously presented) The computer system of claim 45, further comprising computer code that signals an error if said memory access instruction is a read operation and said memory status indicates said memory location is in an allocated-and-uninitialized state.

47. (Previously presented) The computer system of claim 42, wherein said memory status is maintained for said memory location.

48. (Previously presented) The computer system of claim 42, wherein said second set of machine instructions has additional memory monitoring instructions of substantially all memory access instructions that access a region of memory.

49. (Previously presented) The computer system of claim 42, wherein said first and second set of machine instructions are object code.